Using the Intersil X5165, X5325, X5645 CPU Supervisors with the 8051 Microcontroller

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Introduction

This Intersil CPU Supervisors feature a low voltage reset controller, a programmable watchdog timer, and from 16K bits to 64K bits of serial EEPROM in a single package. Although these devices can be used to with practically any microcontroller, the 8051 is used here to demonstrate the operation.

Implementation

The circuit shown in Figure 1 illustrates the connection of the CPU Supervisor to the 8051 microcontroller. The ports shown in this figure correspond to the software routines in the related assembly code. The following are routines provided for implementing an interface to these devices.

wren_cmd – This command routine sets the write enable latch. this latch must be set before (and is automatically reset after) writing to either the EEPROM memory array or the status register.

wrdi_cmd – This command routine resets the write enable latch.

wrsr_cmd – This command routine writes the watchdog timeout period bits (WD0, WD1) and the Block Protect bits (BP0, BP1) in the status register.

rdsr_cmd – This command routine reads the status register.

byte_write – This command routine writes a single byte to the EEPROM memory array.

byte_read – This command routine reads a single byte from the EEPROM memory array.

page_write – This command routine writes 3 consecutive bytes to the EEPROM memory array. It can easily be modified to write an entire page (maximum of 4 bytes).

sequ_read – This command routine reads three consecutive bytes from the EEPROM memory array. It can be easily modified to read any number of bytes.

rst_wdog – This routine is used to reset the watchdog timer without sending a command.

More Information

Additional code can be found on the Intersil website site at http://www.intersil.com.

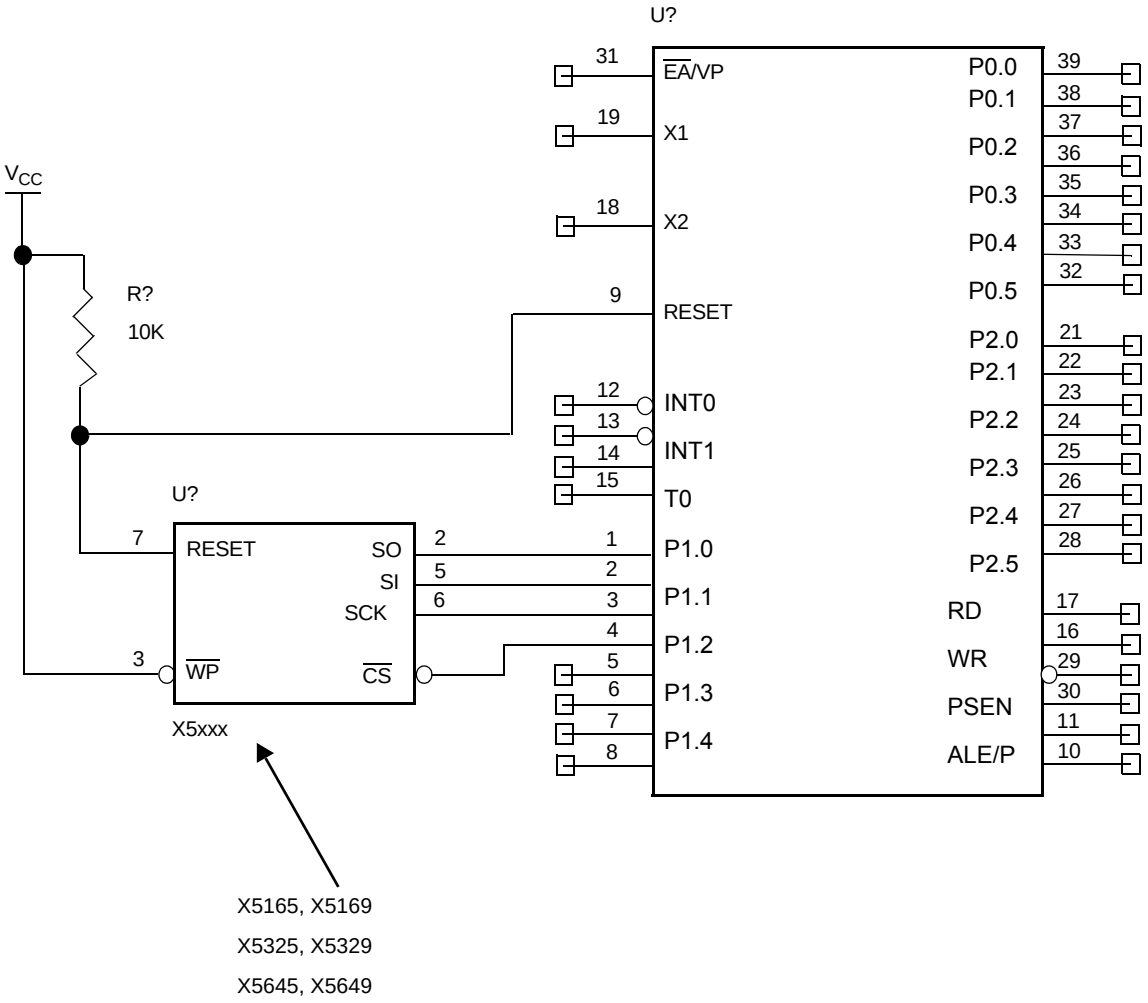

FIGURE 1. INTERFACE OF 8051 TO INTERSIL CPU SUPERVISOR